ESD EDA Verification Flow Applied to Smart Power IC's

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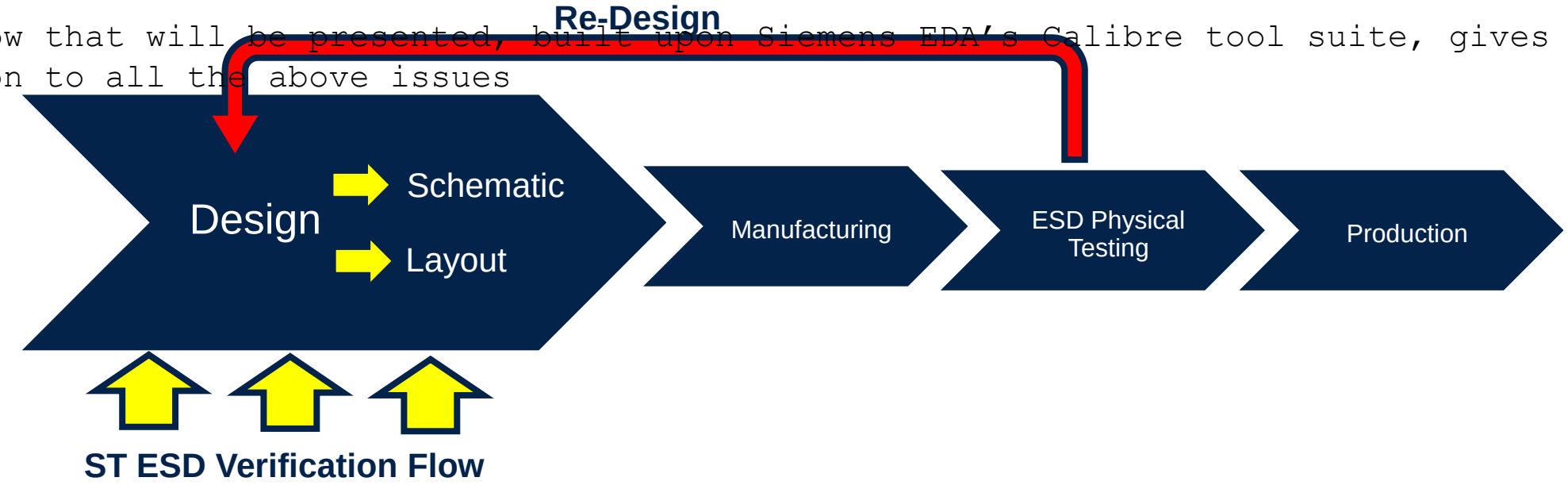
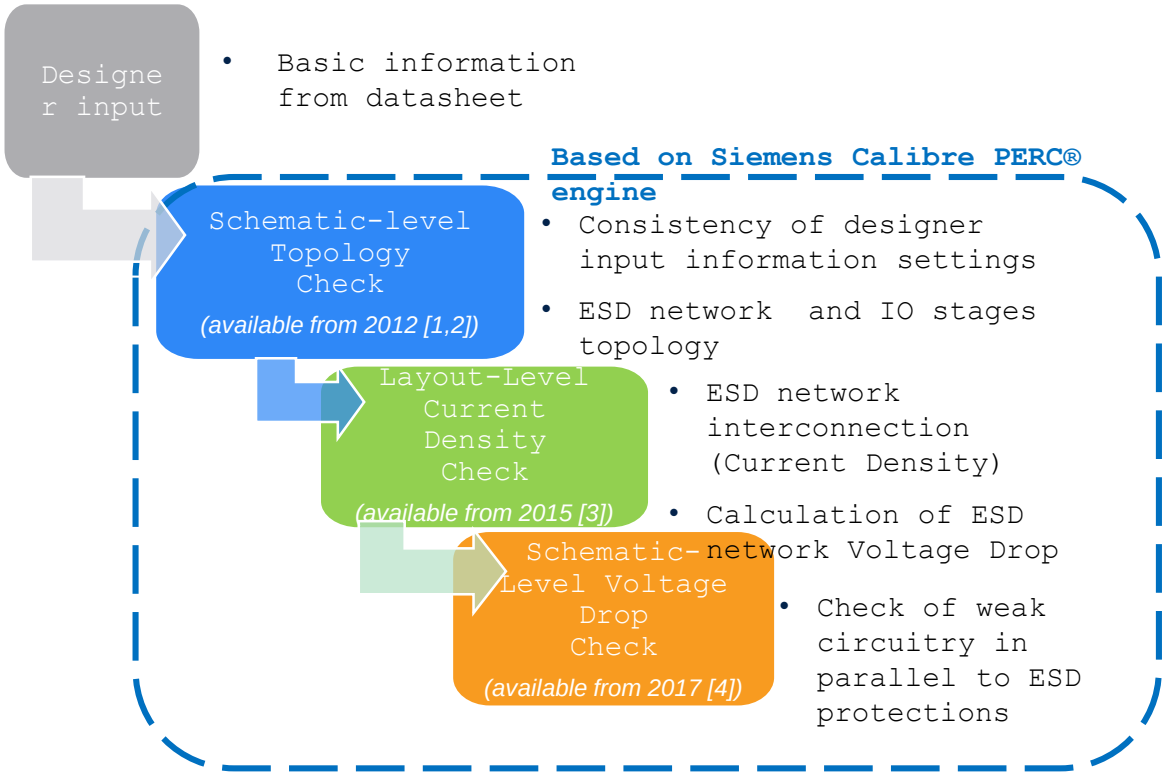
Why do we need efficient ESD checks on design

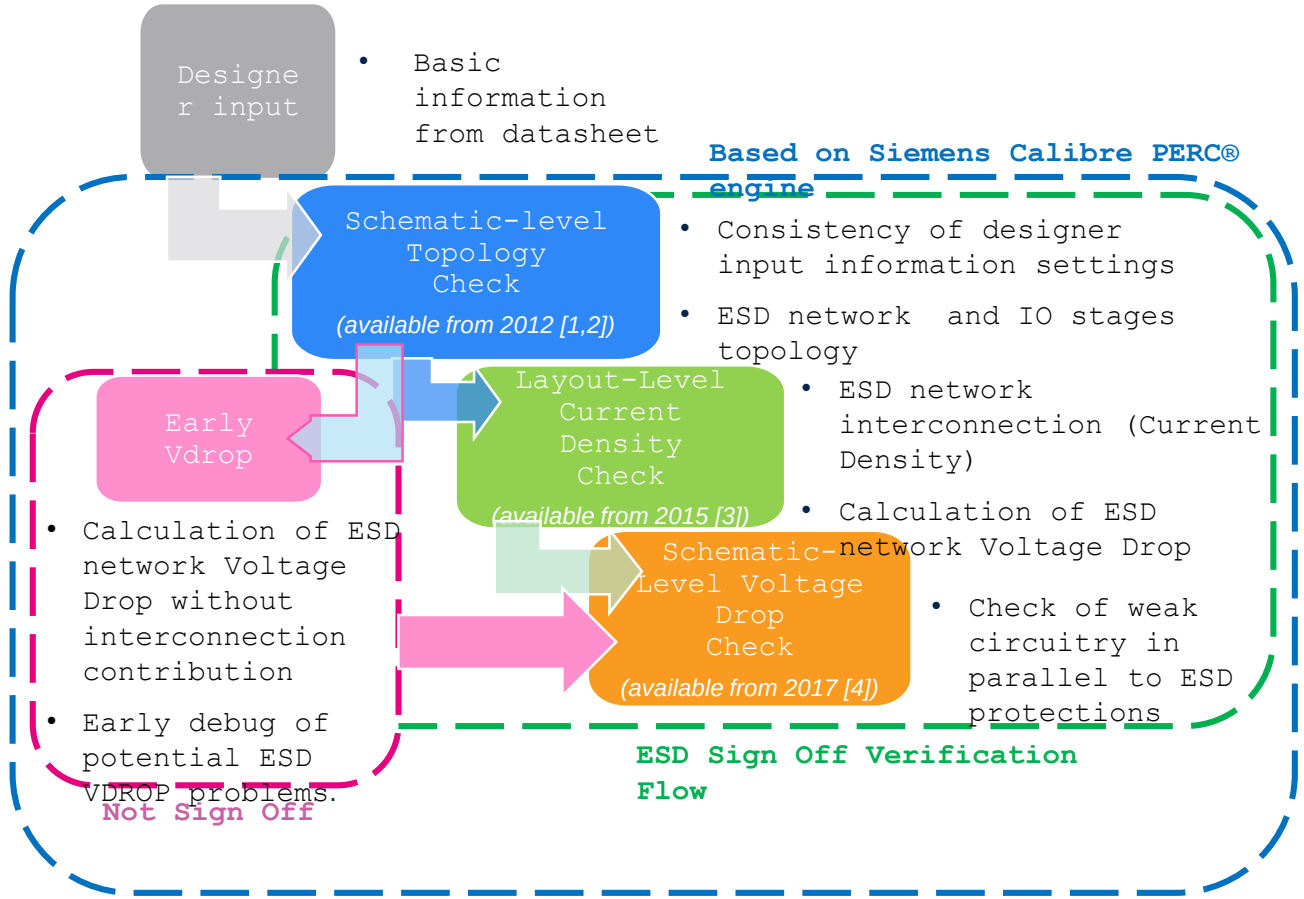
- ESD phenomenon can damage any product during manufacturing phase
- Products need to be built robust against ESD before production
- ST ESD workflow is performed at design level (schematic & layout). It detects all issues that may arise during physical testing and prevents redesign → reach product ESD validation asap (money, time, commitment to customer)
- ST ESD workflow can be used at any hierarchical level of the design: cell, IP, ESD ring, full chip level
- **NEW!** Any violation detected during layout validation can be costly to correct, but with the new **EVDROP tool** it is possible to perform a preliminary assessment of ESD network effectiveness at the schematic level and significantly limit such cases
- The flow that will be presented, built upon Siemens EDA's Calibre tool suite, gives a solid solution to all the above issues



ESD SIGN-OFF Flow

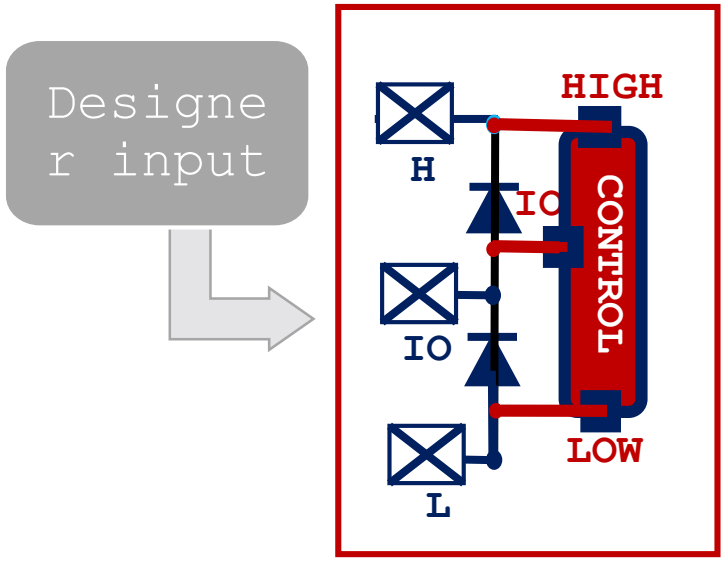


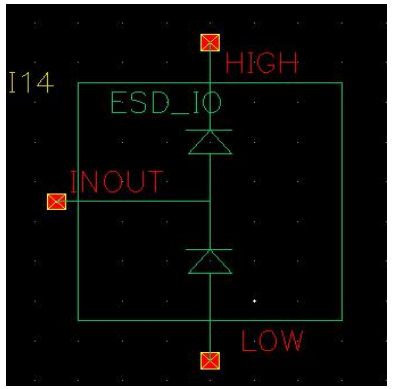
Improved ESD Checking Flow with in-Design capability



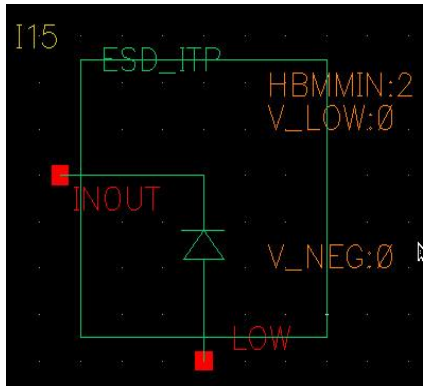
- [1] M. Fragnoli, E.Gevinti, A.Bogani, L.Cerati, "Novel Initialization and Implementation Method for HBM ESD Compliance Automated Check on Smart Power IC's", DAC 2012
- [2] E. Gevinti et al., "HBM ESD EDA Check Method Applied to Complete Smart Power IC's - Functional Initialization and Implementation", Proc. EOS/ESD Symposium 2013
- [3] E. Gevinti et al., "Schematic-Level and Layout-Level ESD EDA Check Methodology Applied to Smart Power IC's – Initialization and Implementation", Proc. EOS/ESD Symposium 2015

Flow Initialization: Controllers

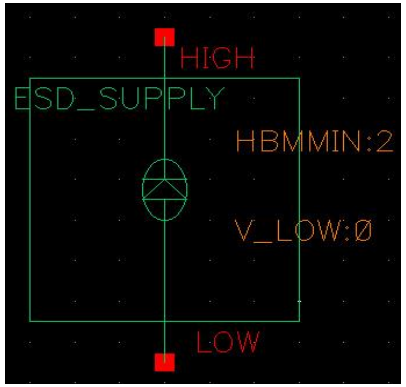




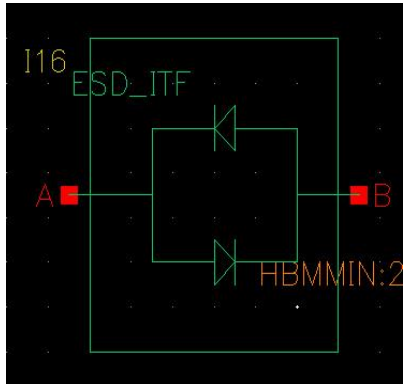
ESD_IO



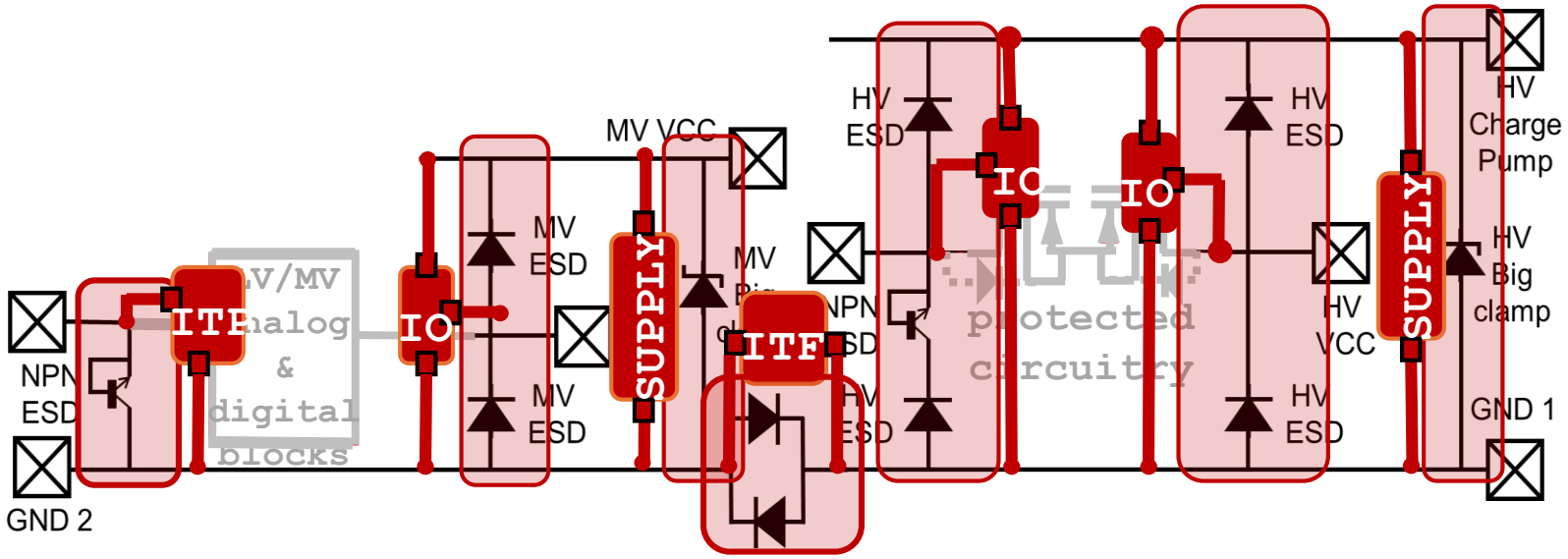
ESD_ITP



ESD_SUPPLY



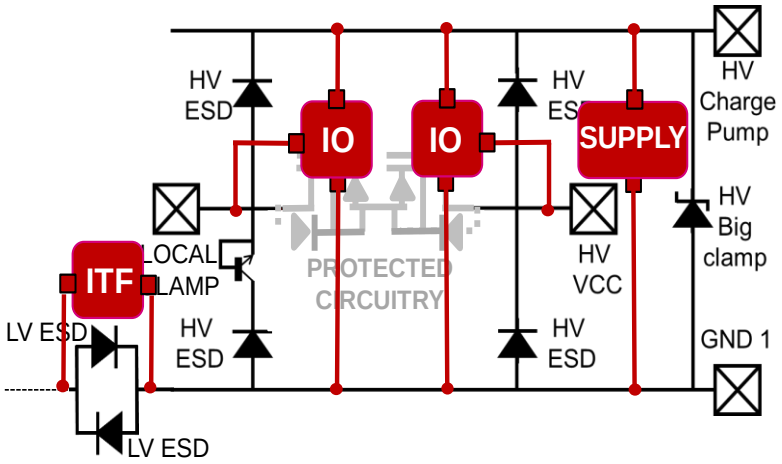
ESD_ITF



- There are 4 "controller" components included into Physical Design Kit
- Controllers need to be placed in schematic view
- Terminals should be connected to the nets to be controlled
- Properties window has to be filled in
- Controller → ESD configuration

From Schematic to Layout Verification

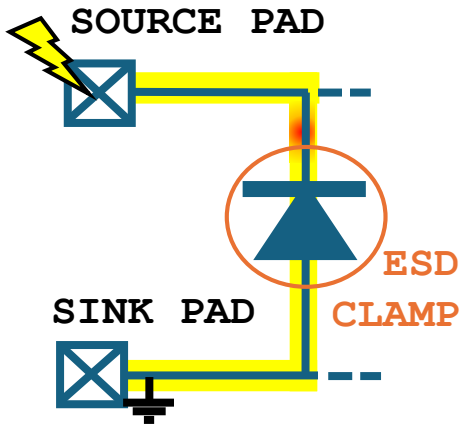
Schematic-level Integrity Check



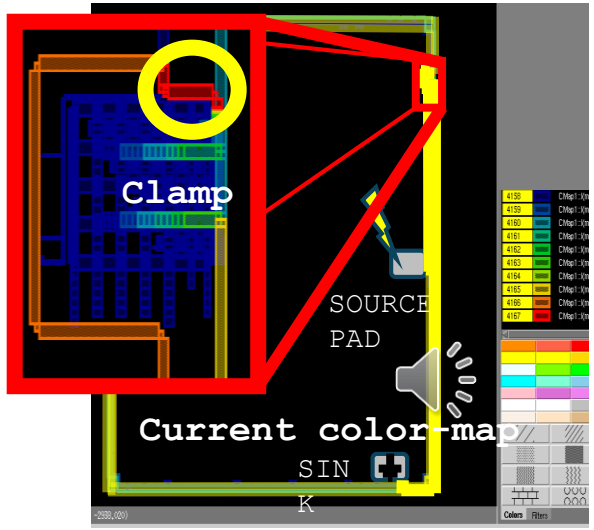
Source Pad	Sink Pad	HBM stress (kV)
IO_x	GND	2
IO_x	VCC	2
VCC	GND	2
…	…	2
IO_GLO	GND	4

- Extracting from schematic each pin functionality (IO / power)
- Information extracted by controllers
- Creating HBM stress pin pairs combination matrix
- Performing all required zaps

Layout-Level Current Density Check



Source	A	Sink	B	**MaxValue**	2.004	HBM	2
Source	C	Sink	D	**MaxValue**	2.356	HBM	2
Source	E	Sink	F	**MaxValue**	1.500	HBM	4



Schematic-level Integrity Check → Early Vdrop Checks

Early Vdrop FLOWCHART

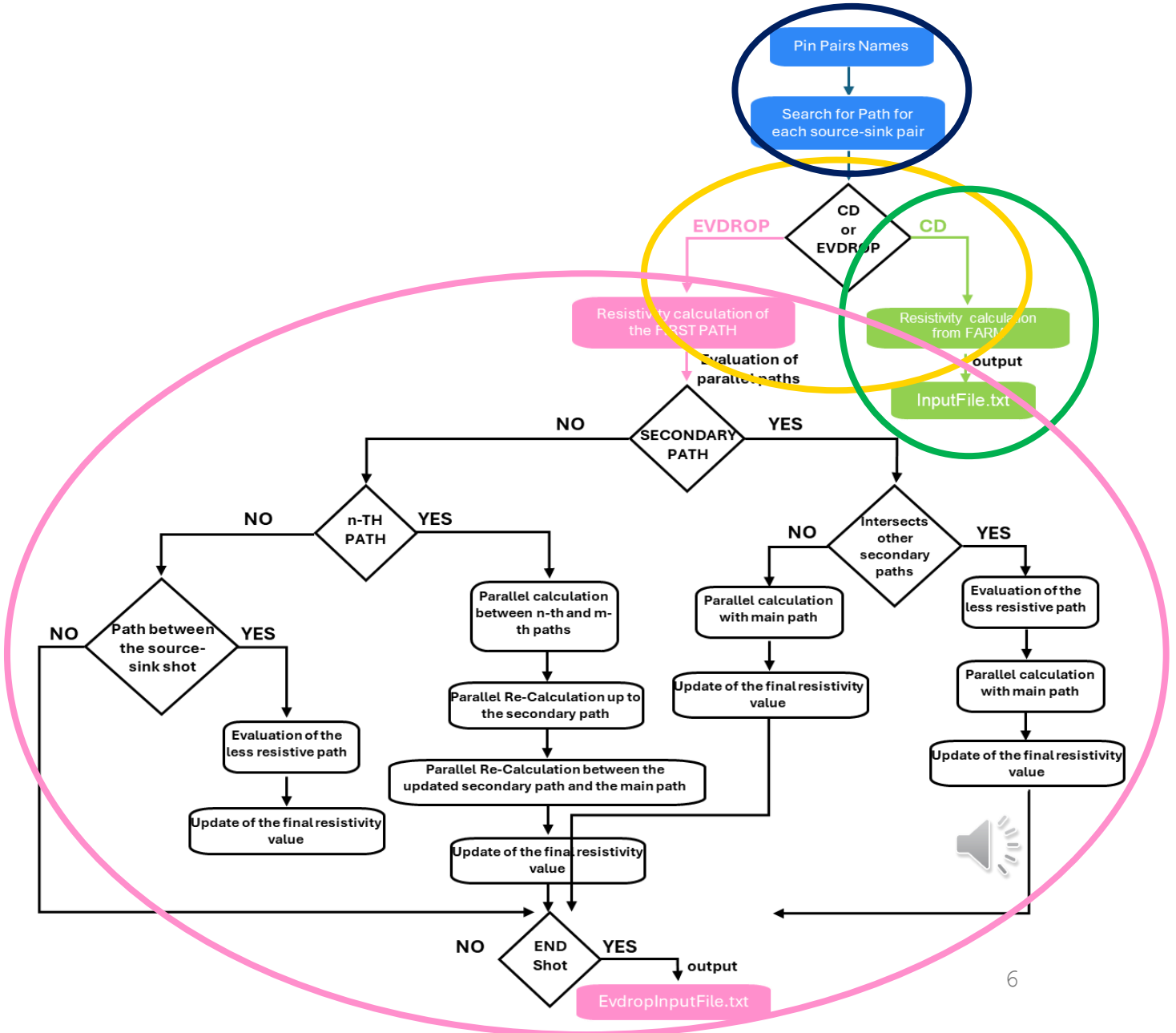
Source	A	Sink	B	**MaxValue**	2.004	HBM	2
Source	C	Sink	D	**MaxValue**	2.356	HBM	2
Source	E	Sink	F	**MaxValue**	1.500	HBM	4

The path search engine is shared by both CD and EARLY VDROP tools. They differ in the calculation of pin-to-pin equivalent resistance for each ESD discharge emulation.

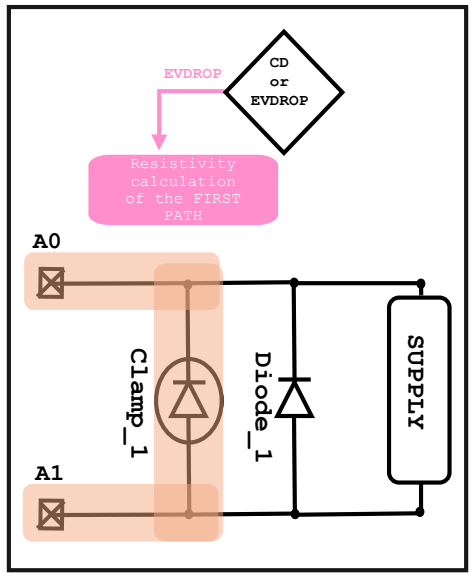
Differences in the two voltage drop output files encompass 3 elements of discrepancy:

1) The metallization contribution

2) The netlist extraction by layout vs. schematic tool

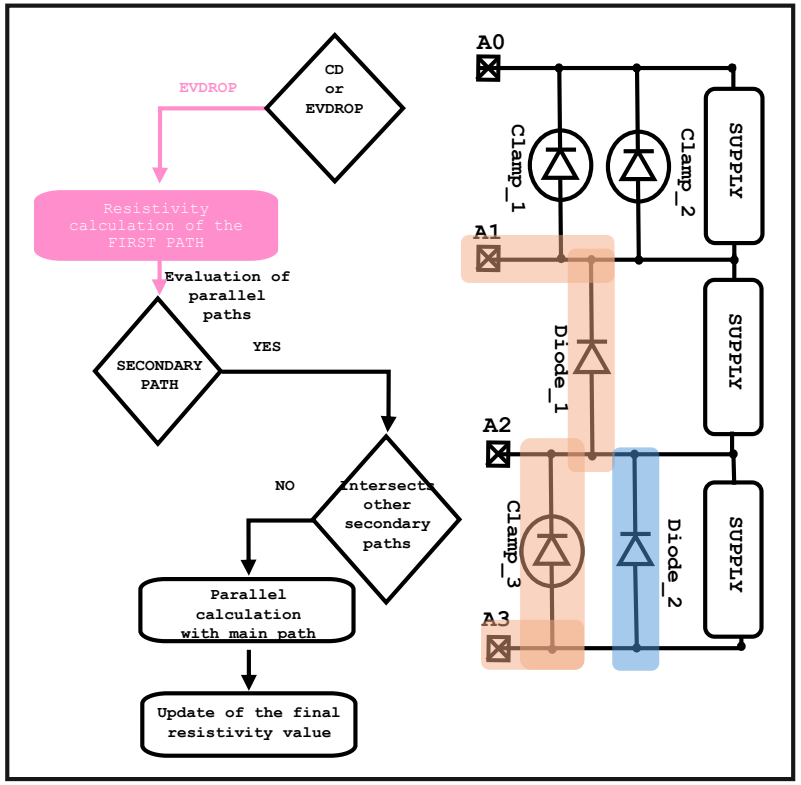


HOW IT WORKS



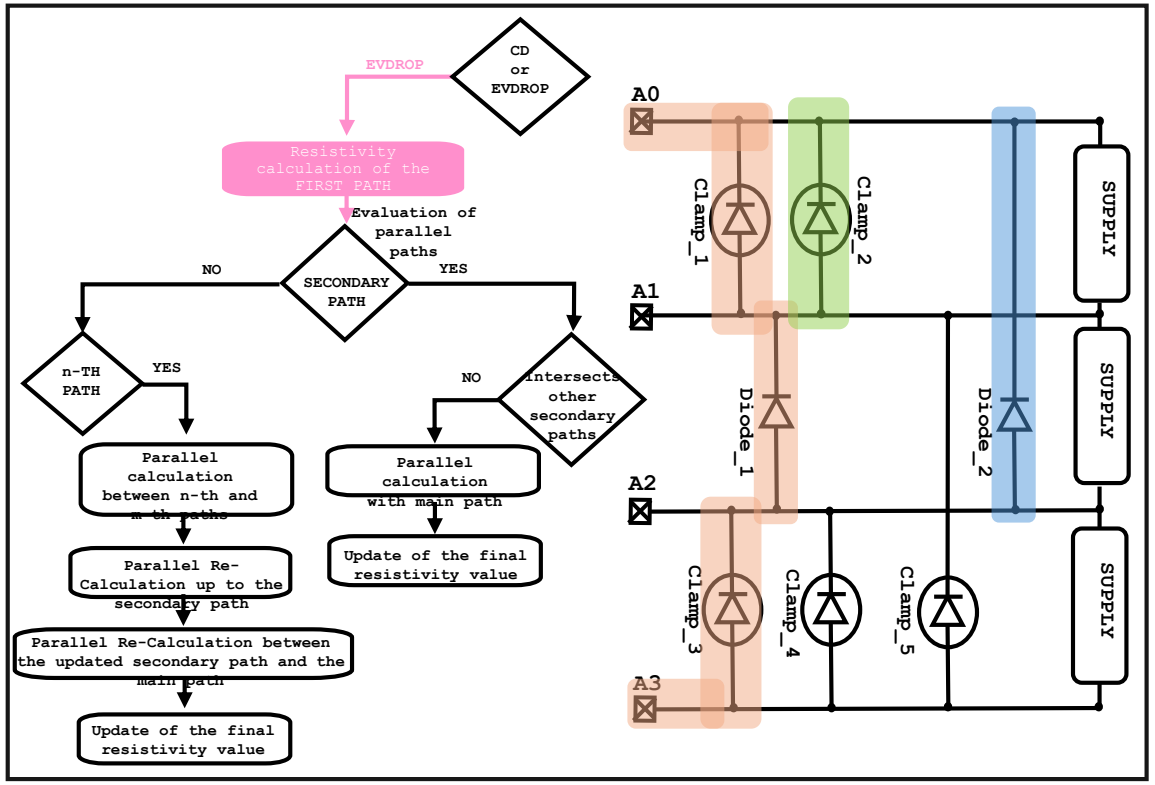
FIRST PATH: A0 → A1

first path evaluated between source-sink pair



FIRST PARH: A3 → A1 + SECONDARY PATH: A3 → A2

path partially parallel to the first one with entry or exit nets different from the source or sink

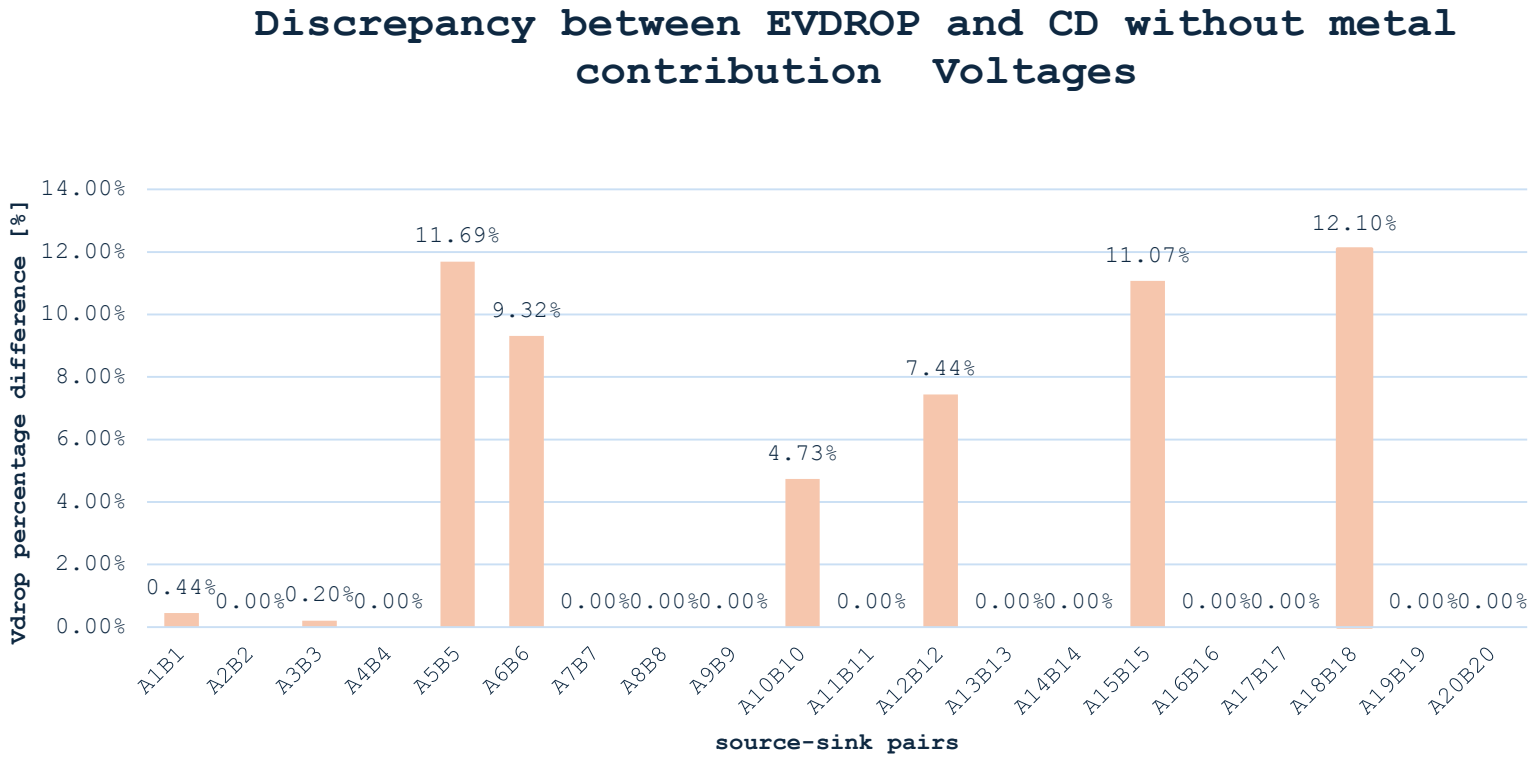


FIRST PARH: A3 → A0 + N-TH PATH: A2 → A0 + A1 → A0

path parallel to m-th path, which in turn may be parallel to other paths but ultimately one of these paths will be parallel to the secondary one

RESULTS ANALYSIS ON A COMPLETE PRODUCT

Source	Sink	Vdrop Percentage Difference	Number of Parallel Paths
A1	B1	0.44%	2
A2	B2	0.00%	Single path
A3	B3	0.20%	2
A4	B4	0.00%	Single path
A5	B5	11.69%	17
A6	B6	9.32%	8
A7	B7	0.00%	Single path
A8	B8	0.00%	Single path
A9	B9	0.00%	Single path
A10	B10	4.73%	4
A11	B11	0.00%	Single path
A12	B12	7.44%	9
A13	B13	0.00%	Single path
A14	B14	0.00%	Single path
A15	B15	11.07%	12
A16	B16	0.00%	Single path
A17	B17	0.00%	Single path
A18	B18	12.10%	13
A19	B19	0.00%	Single path
A20	B20	0.00%	Single path



CD vs EVDROP 3 elements of discrepancy:

1) Metallization contribution cannot be completely removed from the CD evaluation because of the parallel interconnection of parallel devices in layout.
2) Netlist extraction by layout vs. schematic
3) The resistivity calculation by Calibre CD tool vs. EVDROP custom tool

We can confidently state that the tool's results are very promising, making it a highly effective solution that will

Conclusions

- ESD checking flow for BCD ST products is a well assessed strategy which has led to tape out hundreds of products releases in the latest years, with positive ESD results during IC qualification

- The EVDROP tool is a support tool to standard verification flow, that operates way before the layout design phase
  - It proactively identifies voltage drop issues along ESD discharge paths
  - Tool results are very promising, making it a highly effective solution that is expected to reduce ESD design verification cycle time and development costs